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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/322,708	05/28/1999	KIRK DOW SANDERS	81862.P125	8389
8791	791 7590 11/19/2004		EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR			HO, DUC CHI	
			ART UNIT	PAPER NUMBER
LOS ANGELI	ES, CA 90025-1030		2665	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)			
Office Action Summary		09/322,708	SANDERS ET AL.			
		Examiner	Art Unit			
		Duc C Ho	2665			
Period fo	The MAILING DATE of this communication ap or Reply	pears on the cover sheet with the o	orrespondence address			
THE - Exte after - If the - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLEMAILING DATE OF THIS COMMUNICATION. Insions of time may be available under the provisions of 37 CFR 1. SIX (6) MONTHS from the mailing date of this communication. In period for reply specified above is less than thirty (30) days, a replay period for reply is specified above, the maximum statutory period period for reply within the set or extended period for reply will, by statuting reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).		nely filed rs will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).			
Status						
1)	Responsive to communication(s) filed on 04 A	August 2004				
2a)⊠		s action is non-final.				
3)	· /—					
·	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Dispositi	on of Claims					
5)⊠ 6)⊠ 7)□	Claim(s) <u>1-37</u> is/are pending in the application 4a) Of the above claim(s) is/are withdra Claim(s) <u>10-37</u> is/are allowed. Claim(s) <u>1-9</u> is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or	awn from consideration.				
Applicati	on Papers					
9)	The specification is objected to by the Examine	er.				
	10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.					
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
440	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).					
11)	The oath or declaration is objected to by the E	xaminer. Note the attached Office	Action or form PTO-152.			
Priority u	ınder 35 U.S.C. § 119					
a)[Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority documen 2. Certified copies of the priority documen 3. Copies of the certified copies of the priority application from the International Burea see the attached detailed Office action for a list	ts have been received. ts have been received in Applicationity documents have been received in (PCT Rule 17.2(a)).	on No ed in this National Stage			
Attachment		<u>_</u>				
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail Da				
3) 🔲 Inforn	e of Dransperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 'No(s)/Mail Date		atent Application (PTO-152)			

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Claim Rejections - 35 USC § 112

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1. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the amended limitation "without transferring the plurality unused fields of the TDM stream to a network coupled to the transmission system" in lines 8-9 lacks support from the specification. The same remark applies to claim 6, lines 10-11.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Pitroda et al.(US 4,149,038), hereinafter referred as Pitroda.

Pitroda discloses a method and apparatus for fault detection in PCM multiplexed system.

receiving a time division multiplexed (TDM) stream on an input of the transmission system, wherein the TDM stream comprises a plurality of data fields (busy data channels) and a plurality of unused fields (idle channels) (a logic circuit 47-fig. 3 for receiving a TDM stream including busy data channels and idle channels, see col. 11, lines 23-25);

inserting test data in one or more of the plurality unused fields of the TDM stream using a logic circuit (circuit 47-fig. 3 inserts bit patterns (all "0's" and all "1's" patters) into idle channels (col. 13, lines 33-41))

transferring the TDM stream along a plurality of components of the transmission system, and back to the logic circuit (transfer the TDM from circuit 47 through a plurality channels (col. 13, lines 33-41) and transfer the TDM from circuit 47 through a plurality of components (mux/demux and switching network shown in fig. 2) and back to circuit 47 (col. 14, lines 35-42)).

comparing the test data against the transferred data using the logic circuit (Circuit 47 compares the all "0's" or all "1's" patterns with the received test patterns (col. 15, lines 5-34). The comparison is performed by the comparator 322 (figure 4) in circuit 47 as described in col. 22, lines 60-66).

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Regarding claim 2, the connection path for transferring the TDM stream in the Pitroda is the mux/demux and switching network shown in fig. 2.

Regarding claim 3, one or more of the idle channels is(are) used in the connection path for transferring the TDM stream, see fig. 2.

Regarding claim 4, the transferred test data prior to comparing stored in the register 304, see col. 22-line 56 to col. 23-line 15.

Regarding claim 5, generating an error bit is equivalent to the claimed limitation of generating an error flag, see col. 22-line 56 to col. 23-line 15.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Pitroda, in view of Hilton et al. (US 6,185,594), hereinafter referred to as Hilton.

Pitroda discloses a method and apparatus for fault detection in PCM multiplexed system.

receiving a time division multiplexed (TDM) stream on an input of the transmission system, wherein the TDM stream comprises a plurality of data fields (busy data channels) and a plurality of unused fields (idle channels) (a logic circuit 47-fig. 3 for receiving a TDM stream including busy data channels and idle channels, see col. 11, lines 23-25);

inserting test data in one or more of the plurality unused fields of the TDM stream using a logic circuit (circuit 47-fig. 3 inserts bit patterns (all "0's" and all "1's" patters) into idle channels (col. 13, lines 33-41))

transferring the TDM stream along a plurality of components of the transmission system, and back to the logic circuit (transfer the TDM from circuit 47 through a plurality channels (col. 13, lines 33-41) and transfer the TDM from circuit 47 through a plurality of components (mux/demux and switching network shown in fig. 2) and back to circuit 47 (col. 14, lines 35-42)).

comparing the test data against the transferred data using the logic circuit (Circuit 47 compares the all "0's" or all "1's" patterns with the received test patterns (col. 15, lines 5-34). The comparison is performed by the comparator 322 (figure 4) in circuit 47 as described in col. 22, lines 60-66).

Pitroda, however, doesn't specifically teach generating a test signal, wherein the test signal is generated by the DSP.

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One skilled in the art would recognize the advantage of using a test signal generated by a Digital Signal Processing (DSP) chip.

Hilton discloses a versatile signal generator. In Hilton, DSP chips are capable of generating test signals, see col. 2, lines 33-42.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ the DSP chip for generating test signals as taught by Hilton into the system of Pitroda since the DSP chip can accept a real time input signal and to produce a real time digitally modulated signal, and therefore the combination system of Pitroda and Hilton would provide an efficient model for precisely testing a transmission system with real world conditions as well as known signals that conform to industry standard.

Regarding claim 7, in Pitroda, the connection path for transferring the TDM stream in the Pitroda is the mux/demux and switching network shown in fig. 2.

Regarding claim 8, in Pitroda one or more of the idle channels is(are) used in the connection path for transferring the TDM stream, see fig. 2.

Regarding claim 9, in Pitroda generating an error bit is equivalent to the claimed limitation of generating an error flag, see col. 22-line 56 to col. 23-line 15.

Allowable Subject Matter

8. Claims 10-37 are allowed.

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Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTHS shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136 (a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Ho whose telephone number is (571) 272-3147. The examiner can normally be reached on Monday through Friday from 7:00 am to 3:30 pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

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The fax phone number for the organization where this application or proceeding

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is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner

Duc Ho

11-10-04